SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a small size semiconductor package, and more particularly, to a semiconductor package of substantially the same size ~~of~~ as a semiconductor ~~device~~ chip referred to as a chip size package, a semiconductor device using the semiconductor device, and a manufacturing method of the semiconductor device.

2. Description of the Related Art

These days, various apparatus including semiconductor devices, particularly portable apparatus and movable apparatus are being miniaturized and lightened. Semiconductor devices for use in these apparatus are thus desired to be miniaturized and lightened accordingly.

In order to meet the demands, a package of substantially the same ~~side of~~ size as a semiconductor ~~device~~ chip referred to as a chip size package (hereinafter referred to as CSP) has recently been proposed, and some semiconductor devices using such a chip size package are implemented as products.

As a semiconductor device formed with a semiconductor

~~element~~ Chip mounted on a CSP, for example, as shown in Fig. 8, one in which a semiconductor ~~element~~ Chip 3 is mounted and fixed via bumps 2 on a semiconductor package 1 is known. In this semiconductor device, the semiconductor package 1 comprises a substrate 4, a conductive connecting pattern 5 formed on one side of the substrate 4, a conductive connecting pattern 6 formed on the other side of the substrate 4, and a wiring material 7 formed so as to pierce the substrate 4 for the purpose of making the connecting pattern 5 electrically connected to the connecting pattern 6. As the material of the substrate 4, ceramics are mainly used for the purpose of making smaller the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ Chip 3 and the substrate 4 and thus making smaller the thermal stress to be applied to the bumps 2 and the semiconductor element 3.

The semiconductor ~~element~~ Chip 3 is fixed to the substrate 4 of the semiconductor package 1 thus structured with the conductive connecting pattern 5 formed on the one side of the substrate 4 being electrically connected thereto via the bumps 2 provided on a surface 3a where the element is formed. External connecting terminals 8 such as solder balls for bonding the conductive connecting pattern 6 to a mother board (not shown) are

fixed to the conductive connecting pattern 6 formed on the other side of the substrate 4. By this, the bumps 2 of the semiconductor ~~element~~ chip 3 are electrically connected to the external connecting terminals 8 via the connecting pattern 5, the wiring material 7, and the connecting pattern 6.

The semiconductor ~~element~~ chip 3 thus mounted on the semiconductor package 1 is integrally fixed to the semiconductor package 1 by sealing the whole periphery of the junction between the substrate and the semiconductor ~~element~~ chip 3 with resin 9 referred to as underfile. It is to be noted that the resin 9 referred to as underfile also performs a function to disperse the above-mentioned thermal stress due to the difference of the coefficient of thermal expansion between the substrate 4 and the semiconductor ~~element~~ chip 3.

Fig. 9 illustrates another example of a semiconductor device formed with a semiconductor element mounted on a CSP. In Fig. 9, a semiconductor device 10 is generally referred to as a chip on board (COP). The semiconductor device 10 is formed by mounting and fixing a semiconductor ~~element~~ chip 13 via adhesive 12 or the like on a semiconductor package 11.

The semiconductor package 11 comprises a substrate 14 the material of which is glass epoxy resin or the like, a conductive

connecting pattern 15 formed on one side of the substrate 14, a conductive connecting pattern 16 formed on the other side of the substrate 14, and a wiring material 17 formed so as to pierce the substrate 14 for the purpose of making the connecting pattern 15 electrically connected to the connecting pattern 16.

A surface opposite to a surface 13a where the element is formed of the semiconductor ~~element~~ chip 13 is fixed with the adhesive 12 to one side of the substrate 14 of the semiconductor package 11 thus structured. Further, an electrode (not shown) formed on the surface 13a where the element is formed of the semiconductor ~~element~~ chip 13 is electrically connected to the connecting pattern 15 of the semiconductor package 11 via wires 18. External connecting terminals 19 such as solder balls for bonding the conductive connecting pattern 16 to a mother board (not shown) are fixed to the conductive connecting pattern 16 formed on the other side of the substrate 14. By this, the electrodes of the semiconductor ~~element~~ chip 13 are electrically connected to the external connecting terminals 19 via the connecting pattern 15, the wiring material 17, and the connecting pattern 16. The semiconductor package 11 with the semiconductor ~~element~~ chip 13 thus mounted thereon is further provided with resin 20 covering the one side of the substrate 14 and the semiconductor ~~element~~ chip 13 for

the purpose of protecting the surface 13a where the element is formed and the wires 18. By this, the semiconductor ~~element~~ Chip 13 and the wires 18 are sealed with the resin 20.

However, with the semiconductor device shown in Fig. 8, in order to decrease the thermal stress between the substrate 4 and the semiconductor ~~element~~ Chip 3, ceramics, which are expensive, have to be used as the material of the substrate 4, leading to high cost as a whole, which is a problem to be solved.

Further, with the semiconductor device 10 shown in Fig. 9, although, since the thermal stress between the substrate 14 and the semiconductor ~~element~~ Chip 13 can be absorbed by the wires 18, glass epoxy resin, which is inexpensive, can be used as the material of the substrate 14, since the wires 18 are disposed so as to go around to the outer peripheral side of the semiconductor ~~element~~ Chip 13 in this structure, the size of the semiconductor device 10 as a whole with respect to the semiconductor ~~element~~ Chip 13 is large, and thus, the semiconductor device 10 can not sufficiently meet the demands for miniaturizing and thinning the semiconductor device.

SUMMARY OF THE INVENTION

The present invention is made in view of the above, and therefore an object of the invention is to provide a

a semiconductor device which is of substantially the same size ~~of~~ as a semiconductor ~~element~~ chip, which thus sufficiently ~~meeting~~ meets the demands for miniaturizing and thinning the semiconductor device, and which, at the same time, can be manufactured at a low cost, a manufacturing method thereof, and a semiconductor package suitably used in manufacturing the semiconductor device.

According to one aspect of the present invention, in order to solve the above-mentioned problem, a semiconductor package is comprised of a substrate for mounting a semiconductor ~~element~~ chip thereon to fix the side of a surface where the element is formed of the semiconductor ~~element~~ chip to one side thereof, and a connecting pattern provided on the other side of the substrate for electrical connection to the semiconductor ~~element~~ chip, the substrate being provided with a ~~through hall~~ elongate opening formed from the one side to the other side of the substrate.

With this semiconductor package, since a ~~through hall~~ elongate opening is formed in the substrate and the connecting pattern is provided on the side of the substrate opposite to the side on which the surface where the ~~element~~ chip is formed of the semiconductor element is mounted, an electrode formed on the surface where the element is formed of the semiconductor ~~element~~ chip and the connecting pattern can be bonded with wires through the ~~through hall~~ elongate opening. Accordingly,

wires can be disposed without going around to the outer peripheral side of the semiconductor ~~element~~ chip. This eliminates the necessity of securing space for the wires on the outer peripheral side of the semiconductor element.

Further, since wire bonding can be carried out, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ chip and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate.

According to another aspect of the present invention, in order to solve the above-mentioned problem, in a semiconductor device, a semiconductor package is comprised of a substrate for mounting a semiconductor ~~element~~ chip thereon to fix the semiconductor ~~element~~ chip to one side thereof, and a connecting pattern provided on the other side of the substrate, the substrate being provided with a ~~through hall~~ elongate opening formed from the one side to the other side of the substrate, a surface where the element is formed of the semiconductor ~~element~~ chip being mounted on the one side of the substrate, an electrode of the semiconductor ~~element~~ chip being fixed to the one side so as to be within the ~~through hall~~ elongate opening and being electrically connected to the connecting pattern via wires through the ~~through hall~~ elongate opening, and the through hall and the wires

being sealed with resin.

With this semiconductor device, since the semiconductor package of the present invention described above is used, and the electrode formed on the surface where the element is formed of the semiconductor ~~element~~ chip and the connecting pattern of the substrate are bonded with wires through the ~~through hall~~ elongate opening, the wires can be disposed without going around to the outer peripheral side of the semiconductor ~~element~~ chip. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor ~~element~~ chip.

Further, since the semiconductor ~~element~~ chip and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ chip and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate.

According to still another aspect of the present invention, in order to solve the above-mentioned problem, a method of manufacturing a semiconductor device is comprised of the steps of preparing a semiconductor package structured by providing a substrate for mounting a semiconductor ~~element~~ chip thereon to fix the semiconductor ~~element~~ chip to one side thereof and

a connecting pattern provided on the other side of the substrate and by forming a ~~through hall~~ elongate opening from the one side to the other side of the substrate, fixing a surface where the element is formed of the semiconductor ~~element~~ chip on the one side of the substrate of the semiconductor package such that an electrode of the semiconductor ~~element~~ chip is within the ~~through hall~~ elongate opening, electrically connecting the connecting pattern and the electrode of the semiconductor ~~element~~ chip via wires through the ~~through hall~~ elongate opening, and sealing the through hall and the wires with resin.

With this method of manufacturing a semiconductor device, since the semiconductor package of the present invention described above is used, and the electrode formed on the surface where the ~~element~~ chip is formed of the semiconductor element and the connecting pattern of the substrate are bonded with wires through the ~~through hall~~ elongate opening, the wires can be disposed without going around to the outer peripheral side of the semiconductor ~~element~~ chip. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor ~~element~~ chip.

Further, since the semiconductor ~~element~~ chip and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ chip and the substrate, which makes it possible

to use an inexpensive resin substrate instead of an expensive ceramics substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a sectional side elevation illustrating a schematic structure of a first embodiment of a semiconductor device according to the present invention;

Fig. 2A and B are perspective views of the semiconductor device shown in Fig. 1 for explaining the structure thereof, and particularly, for explaining the rear surface side of a semiconductor package, and Fig. 2C is a perspective view of the semiconductor device shown in Fig. 1 for explaining the structure thereof, and particularly, for explaining the front surface side of the semiconductor package;

Fig. 3 is a perspective view of a semiconductor ~~element~~ chip illustrating a surface where the element is formed;

Fig. 4 is a perspective view of the semiconductor device for explaining the rear surface side thereof;

Fig. 5 is a perspective view of the semiconductor device for explaining the rear surface side thereof;

Fig. 6 is a sectional side elevation illustrating a schematic structure of a second embodiment of a semiconductor

device according to the present invention;

Fig. 7 is a sectional side elevation illustrating a schematic structure of a third embodiment of a semiconductor device according to the present invention;

Fig. 8 is a sectional side elevation illustrating a schematic structure of an example of a conventional semiconductor device; and

Fig. 9 is a sectional side elevation illustrating a schematic structure of another example of a conventional semiconductor device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail.

Fig. 1 illustrates a first embodiment of a semiconductor device according to a fourth aspect of the present invention. In Fig. 1, reference numeral 30 denotes a semiconductor device, and the semiconductor device 30 is formed by mounting a semiconductor ~~element~~ chip 32 on a semiconductor package 31. It is to be noted that the semiconductor package 31 in the semiconductor device 30 is a first embodiment of a semiconductor package according to the first aspect of the present invention.

In the semiconductor device 30, the semiconductor package

31 comprises a rectangular substrate 33 for mounting the semiconductor ~~element~~ chip 32 thereon to fix the side of a surface 32a where the element is formed of the semiconductor ~~element~~ chip 32 to one side thereof, and a plurality of connecting patterns 34 provided on the other side of the substrate 33. The material of the substrate 33 is glass epoxy resin or the like. As shown in Fig. 2A, a ~~through hall~~ elongate opening 35 is formed along the longitudinal center line of the substrate 33. The ~~through hall~~ elongate opening 35 is formed as a rectangular opening from the one side to which the semiconductor ~~element~~ chip 32 is fixed to the other side. It is to be noted that, as shown in Figs. 1 and 2A, the respective connecting patterns 34 are formed so as to extend from longitudinal edge portions of the substrate 33 to the ~~through hall~~ elongate opening 35, and are made of metal or the like and are conductive.

As shown in Figs. 1 and 2B, an insulating film 36 covering the connecting patterns 34 with the connecting patterns 34 being partly exposed is formed on the other side of the substrate 33 on which the connecting patterns 34 are formed. The insulating film 36 is made of resist or the like, and is provided with end portions 34a of the connecting patterns 34 on the side of the ~~through hall~~ elongate opening 35 and portions other than the end portions 34a, in this example, end portions 34b opposite to the end

portions 34a, exposed, and with the ~~through hall~~ elongate opening 35 left opened, i.e., without covering the ~~through hall~~ elongate opening 35.

As shown in Figs. 1 and 2C, a tape-like bonding material 37 is provided on the one side of the substrate 33 of the semiconductor package 31 thus structured with a portion around the longitudinal center line of the ~~through hall~~ elongate opening 35 being opened. The bonding material 37 is formed by applying thermoplastic adhesive such as polyamideimide or thermosetting adhesive such as modified epoxy resin on both sides of a tape base material made of resin such as polyimide.

As shown in Fig. 1, the semiconductor ~~element~~ chip 32 is mounted and fixed via the bonding material 37 on the one side of the substrate 33. As shown in Fig. 3, the semiconductor ~~element~~ chip 32 is like a rectangular plate with a plurality of electrodes 38 formed on the longitudinal center line of the surface 32a where the element is formed. The electrodes 38 are disposed within the ~~through hall~~ elongate opening 35.

As shown in Figs. 1 and 4, the electrodes 38 of the semiconductor ~~element~~ chip 32 disposed within the through hall 35 are connected to the end portions 34a of the connecting patterns 34 via wires 39 through the ~~through hall~~ elongate opening 35. By this, the electrodes 38 are electrically connected to the connecting

patterns 34.

As shown in Fig. 1, external connecting terminals 40 such as solder balls are connected to the other exposed end portions 34b of the connecting patterns 34. By this structure, the electrodes 38 of the semiconductor ~~element~~ chip 32 are electrically connected to the external connecting terminals 40 via the wires 39 and the connecting patterns 34.

Further, as shown in Figs. 1 and 5, the ~~through hall~~ elongate opening 35 through which the wires 39 for connecting the electrodes 38 to the connecting patterns 34 are disposed is filled with insulating resin 41 covering the end portions 34a of the connecting patterns 34. By this, the electrodes 38, the wires 39, and the end portions 34a of the connecting patterns 34 are sealed and insulated from the external.

Next, a method of manufacturing the semiconductor device 30 thus structured is described. It is to be noted that the example of a manufacturing method described herein is an embodiment according to a seventh aspect of the present invention.

First, the semiconductor package 31 shown in Figs. 2A - C and the semiconductor ~~element~~ chip 32 shown in Fig. 3 are prepared. Here, the tape-like bonding material 37 provided on the one side

of the substrate 33 of the semiconductor package 31 may be provided on the side of the semiconductor ~~element~~ chip 32 instead of being provided on the side of the substrate 33.

Next, the semiconductor ~~element~~ chip 32 is mounted on one side of the semiconductor package 31 thus prepared with the electrodes 38 of the semiconductor ~~element~~ chip 32 being within the ~~through hall~~ elongate opening 35. Next, by heating and pressurizing them with this state maintained, the substrate 33 of the semiconductor package 31 and the surface 32a where the element is formed of the semiconductor ~~element~~ chip 32 are made to closely adhere to each other. By melting and solidifying, or by curing, the adhesive of the bonding material 37, the semiconductor ~~element~~ chip 32 is fixed to the one side of the substrate 33.

Then, as shown in Fig. 4, wire bonding is carried out with respect to the electrodes 38 within the ~~through hall~~ elongate opening 35 in the substrate 33 and the corresponding end portions 34a of the connecting patterns 34 on the other side of the substrate 33. Next, the electrodes 38 are electrically connected to the connecting patterns 34 via the wires 39 through the ~~through hall~~ elongate opening 35. It is to be noted that a conventionally used wire bonder may be used to carry out the wire bonding.

Then, as shown in Fig. 5, the ~~through hall~~ elongate opening 35 is filled

with the insulating resin 41 such as epoxy resin, and the insulating resin 41 is applied so as to cover the wires 38 and the end portions 34a of the connecting patterns 34 to seal all of the electrodes 38, the wires 39, and the end portions 34a of the connecting patterns 34.

After that, the external connecting terminals 40 such as solder balls are bonded to the respective end portions 34b of the connecting patterns 34 under high temperature to obtain the semiconductor device 30.

With the semiconductor device 30 thus obtained, since the electrodes 38 formed on the surface 32a where the element is formed of the semiconductor ~~element~~ Chip 32 and the connecting patterns 34 of the substrate 33 are bonded with the wires 39 through the ~~through hall~~ elongate opening 35, it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor ~~element~~ Chip 32, which leads to miniaturizing and thinning the device as a whole.

Further, since the semiconductor ~~element~~ Chip 32 and the substrate 33 are bonded with the wires, the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ Chip 32 and the substrate 33, which makes it possible to use an inexpensive resin substrate instead of an

expensive ceramics substrate.

Fig. 6 illustrates a second embodiment of a semiconductor device according to the fourth aspect of the present invention. The difference between a semiconductor device 50 in Fig. 6 and the semiconductor device 30 shown in Fig. 1 resides in the structure of a semiconductor package 51 in the semiconductor device 50. The semiconductor package 51 in the semiconductor device 50 is a second embodiment of a semiconductor package according to the first aspect of the present invention. The semiconductor package 51 differs from the semiconductor package 31 shown in Fig. 1 in that its connecting patterns 52 are formed in a plurality of stages (two stages in this example).

More specifically, a substrate 53 of the semiconductor package 51 is formed of an upper plate 53a and a lower plate 53b. The lower plate 53b is formed such that its edge on the side of a elongate opening ~~through hall~~ 54 is outside an edge of the upper plate 53a. By this structure, the rear surface (the other side) of the substrate 53 is formed to be in two stages, i.e., the rear surface of the upper plate 53a and the rear surface of the lower plate 53b.

A first plurality of connecting patterns 52a are provided on the rear surface of the upper plate 53a of the substrate 53.

A second plurality of connecting patterns 52b are provided on the rear surface of the lower plate 53b. The first and the second connecting patterns 52a and 52b are electrically connected to each other via a wiring material 55 provided so as to pierce the lower plate 53b. By this structure, the connecting patterns 52 are in two stages (a plurality of stages) formed by the first connecting patterns 52a, the wiring material 55, and the second connecting patterns 52b.

An insulating film 56 is formed on the rear surface of the lower plate 53b so as to cover the second connecting patterns 52b. It is to be noted that, in this example also, the insulating film 56 is formed with the second connecting patterns 52b being partly exposed, that is, similarly to the one shown in Fig. 2B, with longitudinal end portions of the substrate 53 being exposed.

In the elongate opening ~~through hall~~ 54 formed with the stages in the substrate 53 formed of the upper plate 53a and the lower plate 53b in this way, the electrodes 38 of the semiconductor chip ~~element~~ 32 disposed within the elongate opening ~~through hall~~ 54 are connected via the wires 39 to the end portions of the first connecting patterns 52a exposed on the rear surface of the upper plate 53a of the substrate 53. Further, the elongate opening ~~through hall~~ 54 is filled with

insulating resin 57 covering the wires 39 and the end portions of the first connecting patterns 52a. By this, the electrodes 38, the wires 39, and the end portions of the first connecting patterns 52a are sealed and insulated from the external.

With the semiconductor device 50 thus structured, similarly to the case of the semiconductor device 30 shown in Fig. 1, since it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor ~~element~~ chip 32, the device can be miniaturized and thinned as a whole. Further, since the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ chip 32 and the substrate 53, an inexpensive resin substrate can be used as the substrate 53.

Still further, since the substrate 53 is formed in two stages of the upper plate 53a and the lower plate 53b, and the connecting patterns 52 are in two stages (a plurality of stages) formed by the first connecting patterns 52a, the wiring material 55, and the second connecting patterns 52b, such that the wires 39 are connected to the end portions to the central side of the substrate 53, that is, to the end portions provided on a stage on the side of the one side of the substrate 53, the wires 39 may be cased within the ~~through hall~~ elongate opening 54 without extending to the

outside. By this, the wires 39 can be covered with the insulating resin 57 just by filling the ~~through hall~~ elongate opening 54 with the insulating resin 57 at the bottom of the substrate 53 without heaping up the insulating resin 57 on the rear surface of the lower plate 53b. Accordingly, the diameter of the external connecting terminals 40 such as solder balls can be made small, which leads to finer pitch of the external connecting terminals 40.

Fig. 7 illustrates a third embodiment of a semiconductor device according to the fourth aspect of the present invention. The difference between a semiconductor device 60 in Fig. 7 and the semiconductor device 30 shown in Fig. 1 resides in the structure of a semiconductor package 61 in the semiconductor device 60. The semiconductor package 61 in the semiconductor device 60 is a third embodiment of a semiconductor package according to the first aspect of the present invnetion. The semiconductor package 61 differs from the semiconductor package 31 shown in Fig. 1 mainly in that a plurality of ~~through halls~~ elongate opening 63, two through halls 63 in this example, are formed in a substrate 62.

More specifically, two lines of the ~~through halls~~ elongate openings 63 are formed in the substrate 62 of the semiconductor package 61 along

the longitudinal direction of the substrate 62. Connecting patterns 64 are formed and disposed so as to cross the ~~through~~ elongate openings ~~halls~~ 63 from the outside of the ~~through halls~~ elongate openings 63 (from the longitudinal sides of the substrate 62) to the central side of the ~~through halls~~ elongate openings 63. Outside end portions of the connecting patterns 64 are covered with an insulating film 65 with part of them being exposed toward the outside.

Two lines of electrodes 67 are formed on a surface where the element is formed of a semiconductor ~~element~~ chip 66 mounted on the semiconductor package 61 of the semiconductor device 60. The respective electrodes 67 are disposed within either of the through halls 63 in the substrate 62.

The electrodes 67 are connected to the connecting patterns 64 via the wires 39 through the ~~through halls~~ elongate openings 63. By this, the electrodes 67 are electrically connected to external connecting terminals 68 connected to the end portions of the connecting patterns 64.

Further, the ~~through halls~~ elongate openings 63 are filled with insulating resin 69 covering the wires 39 and the end portions of the connecting patterns 64 on the side connected to the wires 39. By this, the electrodes 67, the wires 39, and the end portions of the connecting patterns 64 are sealed and insulated from the

external.

With the semiconductor device 60 thus structured, similarly to the case of the semiconductor device 30 shown in Fig. 1, since it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor ~~element~~ Chip 66, the device can be miniaturized and thinned as a whole. Further, since the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ Chip 66 and the substrate 62, an inexpensive resin substrate can be used as the substrate 62.

Still further, the semiconductor ~~element~~ Chip 66 in which the electrodes 67 are disposed on the peripheral side instead of the central portion of the semiconductor ~~element~~ Chip 66 as the semiconductor ~~element~~ Chip to be mounted on the semiconductor package 61.

It is to be noted that though the tape-like bonding material 37 is used to fix the semiconductor ~~element~~ Chip on the substrate of the semiconductor package in the embodiments described in the above, the present invention is not limited thereto, and liquid adhesive such as epoxy resin may be used instead of the bonding material 37.

As described in the above, in the semiconductor package

according to s first aspect of the invention, since the ~~through~~ elongate ~~hall~~ opening is formed in the substrate and the connecting pattern is provided on the side of the substrate opposite to the side on which the surface where the element is formed of the semiconductor ~~element~~ chip is mounted, an electrode formed on the surface where the element is formed of the semiconductor ~~element~~ chip and the connecting pattern can be bonded with wires through the ~~through hall~~ elongate opening. Accordingly, wires can be disposed without going around to the outer peripheral side of the semiconductor ~~element~~ chip. This eliminates the necessity of securing space for the wires on the outer peripheral side of the semiconductor ~~element~~ chip, and thus, a semiconductor device using this can be miniaturized and thinned.

Further, since wire bonding can be carried out, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ chip and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate. By this, the cost of the semiconductor device can be lowered.

In the semiconductor device according to the fourth aspect of the invention, since the semiconductor package of the first aspect of the present invention is used, and the electrode

formed on the surface where the element is formed of the semiconductor ~~element~~ chip and the connecting pattern of the substrate are bonded with wires through the ~~through hall~~ elongate opening, the wires can be disposed without going around to the outer peripheral side of the semiconductor ~~element~~ chip. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor ~~element~~ chip, and thus, the device can be miniaturized and thinned as a whole.

Further, since the semiconductor ~~element~~ chip and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ chip and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate. By this, the cost of the semiconductor device can be lowered.

In the method of manufacturing a semiconductor device according to the seventh aspect of the invention, since the semiconductor package of the first aspect of the present invention is used, and the electrode formed on the surface where the element is formed of the semiconductor ~~element~~ chip and the connecting pattern of the substrate are bonded with wires through the ~~through hall~~ elongate opening, the wires can be disposed without going around

to the outer peripheral side of the semiconductor ~~element~~ chip. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor ~~element~~ chip, and thus, the device can be miniaturized and thinned as a whole.

Further, since the semiconductor ~~element~~ chip and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ~~element~~ chip and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate. By this, the cost of the semiconductor device can be lowered.